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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/631,120	07/31/2003	Gerard Chauvel	TI-35486	3950

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EXAMINER	
PETRANEK, JACOB ANDREW	
ART UNIT	PAPER NUMBER
2183	

NOTIFICATION DATE	DELIVERY MODE
09/19/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/631,120	CHAUVEL ET AL.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-11,14-22 and 25-28* is/are rejected.

7)☒ Claim(s) *12,13,23 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 7-28 are pending.

2. The office acknowledges the following papers:

Specification, arguments, and claims filed on 7/9/2007.

Withdrawn objections

3. The specification objections have been withdrawn due to amendment.

Allowable Subject Matter

4. Claims 12-13 and 23-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

New Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 7-11, 14-22, and 25-28 are rejected under 35 U.S.C. §103(a) as being unpatentable over Chung et al. (U.S. 6,950,929).

7. As per claim 7:

Chung disclosed a method, comprising:

Fetching and decoding instructions in a first processor (Chung: Figure 1 elements 125 and 150, column 3 lines 31-35 and lines 46-65 and column 5 lines 13-17)(The coprocessor is the first processor and has fetch and decode abilities.);

Detecting an unsupported instruction that is not executable by the first processor (Chung: Figure 1 element 112, column 3 lines 19-27)(The predecoder detects instructions that are executable by the CPU and not executable by the coprocessor. Thus having the same functionality.);

Executing said unsupported instruction in a second processor (Chung: Figure 1 element 117, column 3 lines 19-27)(Instructions unsupported by the coprocessor are executed by element 117.); and

Providing the first processor with a supported instruction that is executable in the first processor by loading the supported instruction in decode logic of the first processor without the first processor fetching any portion of said supported instruction (Chung: Figure 1 elements 122 and 125, column 5 lines 1-33)(When executing a loop, the instructions are fetched by the first processor into the loop buffer during the first iteration. On the rest of the iterations, it's obvious to one of ordinary skill in the art that the instructions are sent from the loop buffer to the decoder without requiring fetching from main memory.).

8. As per claim 8:

Chung disclosed the method of claim 7 wherein providing the first processor with the supported instruction comprises loading the supported instruction in decode logic of the first processor by accessing a port addressable by the second processor (Chung:

Figure 1 elements 112 and 128, column 3 lines 19-27 and column 5 lines 1-33)(A port is an interface in which data is transferred from one computer to another. The predecoder will send a signal to element 128 via a port to send the loop buffer instruction to the decoder.)

9. As per claim 9:

Chung disclosed the method of claim 7 further comprising detecting patterns of supported and unsupported instructions yet to be executed to determine when to perform said providing the first processor with the supported instruction that is executable in the first processor without the first processor fetching any portion of said supported instruction (Chung: Figure 1 element 112, column 3 lines 19-27)(The predecoder detects a supported instruction of the coprocessor. The predecoder then clocks the coprocessor to select instructions from the loop buffer after the first iteration. Instructions stored in the loop buffer require no fetching to be provided to the decoder.).

10. As per claim 10:

Chung disclosed the method of claim 9 wherein said patterns comprise an unsupported instruction followed by less then a threshold number of consecutive supported instructions before the next unsupported instruction (Chung: Figure 1 element 112, column 3 lines 19-27)(A supported instruction is a coprocessor instruction, while an unsupported instruction is a processor instruction. It's obvious to one of ordinary skill in the art that a processor instruction could follow a coprocessor instruction within a random threshold number.).

11. As per claim 11:

Chung disclosed a system, comprising:

A first processor having fetch logic and decode logic, the first processor fetches supported instructions from memory using said fetch logic and decodes said supported instructions with said decode logic (Chung: Figure 1 elements 125 and 150, column 3 lines 31-35 and lines 46-65 and column 5 lines 13-17)(The coprocessor is the first processor and has fetch and decode abilities.);

A second processor, the second processor executes unsupported instructions (Chung: Figure 1 element 117, column 3 lines 19-27)(Instructions unsupported by the coprocessor are executed by element 117.);

Means for loading a supported instruction in said decode logic of the first processor so that the first processor decodes but does not fetch any portion of the supported instruction (Chung: Figure 1 elements 122 and 125, column 5 lines 1-33)(When executing a loop, the instructions are fetched by the first processor into the loop buffer during the first iteration. On the rest of the iterations, it's obvious to one of ordinary skill in the art that the instructions are sent from the loop buffer to the decoder without requiring fetching from main memory.);

Means for coordinating when said loading the supported instruction in said decode logic of the first processor so that the first processor decodes but does not fetch any portion of the supported instruction occurs (Chung: Figure 1 elements 122 and 125, column 5 lines 1-33)(When executing a loop, the instructions are fetched by the first processor into the loop buffer during the first iteration. On the rest of the iterations, it's

obvious to one of ordinary skill in the art that the instructions are sent from the loop buffer to the decoder without requiring fetching from main memory.).

12. As per claim 14:

Park disclosed the system of claim 11 wherein said means for coordinating when said loading the supported instruction in said decode logic of the first processor so that the first processor decodes but does not fetch any portion of the supported instruction occurs comprises a control program that examines patterns of supported and unsupported instructions yet to be executed and causes the first processor to switch between multiple instruction execution modes according to the patterns (Chung: Figure 1 element 112, column 3 lines 19-27)(The predecoder detects a supported instruction of the coprocessor and unsupported instructions of the coprocessor. This causes a mode change of executing supported instructions on the coprocessor and executing unsupported instructions on the processor.), wherein said loading the supported instruction in the decode logic of the first processor so that the first processor decodes but does not fetch any portion of the supported instruction is one of said multiple instruction execution modes (Chung: Figure 1 elements 122 and 125, column 5 lines 1-33)(When executing a loop, the instructions are fetched by the first processor into the loop buffer during the first iteration. On the rest of the iterations, it's obvious to one of ordinary skill in the art that the instructions are sent from the loop buffer to the decoder without requiring fetching from main memory.);

13. As per claim 15:

Chung disclosed the system of claim 14 wherein said control program runs on the second processor (Chung: Figure 1 element 112, column 3 lines 19-27)(The predecoder is located on the CPU.).

14. As per claim 16:

Claim 16 essentially recites the same limitations of claim 10. Therefore, claim 16 is rejected for the same reasons as claim 10.

15. As per claim 17:

Chung disclosed the system of claim 16, wherein said threshold number is three (Chung: Figure 1 element 112, column 3 lines 19-27)(A supported instruction is a coprocessor instruction, while an unsupported instruction is a processor instruction. It's obvious to one of ordinary skill in the art that a processor instruction could follow a coprocessor instruction within a random threshold number, including the threshold value of 3.).

16. As per claim 18:

Claim 18 essentially recites the same limitations of claim 7. Claim 18 additionally recites the following limitations:

Detecting patterns of supported and unsupported instructions yet to be executed (Chung: Figure 1 element 112, column 3 lines 19-27)(The predecoder detects a pattern of the next instruction to be executed being a coprocessor or processor instruction.).

17. As per claim 19:

The additional limitation(s) of claim 19 basically recite the additional limitation(s) of claim 8. Therefore, claim 19 is rejected for the same reason(s) as claim 8.

18. As per claim 20:

The additional limitation(s) of claim 20 basically recite the additional limitation(s) of claim 9. Therefore, claim 20 is rejected for the same reason(s) as claim 9.

19. As per claim 21:

The additional limitation(s) of claim 21 basically recite the additional limitation(s) of claim 10. Therefore, claim 21 is rejected for the same reason(s) as claim 10.

20. As per claim 22:

Claim 22 essentially recites the same limitations of claim 11. Claim 22 additionally recites the following limitations:

Means for coordinating when said loading the supported instruction in said decode logic of the first processor so that the first processor decodes but does not fetch any portion of the supported instruction occurs comprises a control program that examines patterns of supported and unsupported instructions yet to be executed and causes the first processor to switch between multiple instruction execution modes according to the patterns (Chung: Figure 1 element 112, column 3 lines 19-27)(The predecoder detects a pattern of the next instruction to be executed being a coprocessor or processor instruction. The coprocessor switches execution modes when a coprocessor instruction is detected on the processor.).

21. As per claim 25:

The additional limitation(s) of claim 25 basically recite the additional limitation(s) of claim 14. Therefore, claim 25 is rejected for the same reason(s) as claim 14.

22. As per claim 26:

The additional limitation(s) of claim 26 basically recite the additional limitation(s) of claim 15. Therefore, claim 26 is rejected for the same reason(s) as claim 15.

23. As per claim 27:

The additional limitation(s) of claim 27 basically recite the additional limitation(s) of claim 16. Therefore, claim 27 is rejected for the same reason(s) as claim 16.

24. As per claim 28:

The additional limitation(s) of claim 28 basically recite the additional limitation(s) of claim 17. Therefore, claim 28 is rejected for the same reason(s) as claim 17.

Response to Arguments

25. The arguments presented by Applicant in the response, received on 7/9/2007 are considered persuasive.

26. Applicant argues "Park failed to teach providing the first processor with a supported instruction that is executable in the first processor by loading the supported instruction in decode logic of the first processor without the first processor fetching any portion of said supported instruction" for claims 7 and 18.

This argument is found to be persuasive for the following reason. The examiner agrees that Park fails to not fetch any portion of a coprocessor instruction and fetches part of the coprocessor instruction, while receiving the other part of the coprocessor instruction from the processor. However, due to the amendment, a new ground of rejection has been made.

27. Applicant argues "Park failed to teach means for coordinating when said loading the supported instruction in said decode logic of the first processor so that the first processor decodes but does not fetch any portion of the supported instruction occurs" for claims 11 and 22.

This argument is found to be persuasive for the following reason. The examiner agrees that Park fails to not fetch any portion of a coprocessor instruction and fetches part of the coprocessor instruction, while receiving the other part of the coprocessor instruction from the processor. However, due to the amendment, a new ground of rejection has been made.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

So (U.S. 6,944,746), taught sending coprocessor instructions into the decoder of the coprocessor.

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Luick (U.S. 7,117,389), taught sending floating point instructions from a failed floating point unit to the floating point unit of the other processor core.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner, Art Unit 2183

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